Hybrid-Coupled Planar Resonator (HPCR) Arms Miniaturized Synthesizers

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***Abstract*—Miniaturization and integration of voltage-controlled oscillators (VCOs) at lower microwave frequencies has long been limited by the size of the planar resonator. For the popular 1-8 GHz band, the reported work describes the methodology to shrink multi-octave band VCOs to a mere 0.3x0.3x-0.08 inches, with a companion line of low-cost power-efficient reconfigurable frequency synthesizers that measure just 0.6x0.6x0.1 inches. The typical measured phase noise for 1-8 GHz synthesizer at 10 kHz offset is -90dBc/Hz with operating DC bias 5V, 50 mA. The settling time is less than 1millisecond and not limited to this frequency, can be extended from 1000 MHz to 18 GHz without changing the VCOs layout and topology.**

I. INTRODUCTION

Compact frequency synthesizers fill many needs in modern communications systems. To achieve full-sized performance in miniature packages, this research work describes a line of extremely compact frequency synthesizers that leverage novel hybrid-coupled planar resonator (HPCR) based voltage-controlled-oscillator (VCO) technology for the stability and low noise needed for emerging wideband, high-data-rate wireless communications systems [1]-[8].

The new RoHS-compliant VCOs employ tiny hybrid-coupled planar resonators with a unique evanescent mode electromagnetic (EM) coupling mechanism for improved quality factor (Q), fast tuning, and reduced phase noise. The reported VCOs and synthesizers are validated with discrete components but the design approach lends itself to integrated circuit (IC) formats using CMOS/BiCMOS/SiGe/GaAs technologies. The miniaturize VCOs can match the phase noise performance of much larger, high-Q resonator-based oscillators and, because of their low mass, are relatively immune to high levels of shock, and vibrations.

For the validation of new VCO design approach, printed coupled resonator network is modeled using a 2.5D/3D electromagnetic (EM) simulation software (Ansys/ADS 2008) and incorporated into an optimized nonlinear oscillator circuit to achieve configurability, and low-phase-noise operation over a desired frequency band [8]. The active device is a discrete low-noise silicon-germanium (SiGe) heterojunction-bipolar-transistor (HBT) device. The nonlinear circuit model contains the oscillator's active device, represented by its S-parameters. The active device SiGe HBT is modeled by large-signal S-parameters to better understand the behavior of the device under quasi-linear (low-signal drive level) and nonlinear (large-signal drive level) conditions. The partitioning of the oscillator works quite well, and the combination of the S-parameters and the nonlinear circuit model agrees closely with measured data. The approach also improves the optimization cycles using harmonic balance circuit simulators.

The new HPCR VCOs are designed for reliable performance from -40 to $+85^0$C and are well suited for applications in industrial, military, and commercial systems. Because of the importance of wide bandwidth and low phase noise in modern communication systems, research into the development of the VCOs began with a study into ways of improving quality factor of the printed resonators in compact size. They have been fabricated on low-loss 30-mil-thick dielectric material with dielectric constant of 3.38, and tested from 1to18 GHz for reconfigurable synthesizer applications.

Compact size and low power consumption is the key criteria for reconfigurable frequency synthesizer. Therefore, the motivation of this research work is towards integrable solutions, avoiding costly, bulky, and power hungry YIG-tuned synthesizers. While reviewing classical YIG-tuned high synthesizer architecture, the current HPCR based VCOs technology trend toward increasing the flexibility and functional integration as well as reducing the size and cost.

II. DESIGN THEORY

Design theory for creating frequency synthesizers are diverse, from traditional analog methods using PLLs to direct digital synthesizers (DDS), which rely on high-speed digital – to-analog converters (DACs) to transform digital input words into analog output signals. For comparative analysis and low-cost but high performance synthesizer solutions, different synthesizer architectures along with their main characteristics are described below [9]-[29].

A. Direct Analog Synthesizer (DAS)

Figure (1) shows the block diagram of direct analog synthesizer (DAS), which is conceptualized by mixing the base frequencies followed by switched filter networks. The base frequency sources are extracted from high Q-factor

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resonator based oscillators (crystal oscillators), which improves the performances of the DAS in terms of phase noise and switching speed but at the cost of step-size, complexity and overall component counts. The alternative solution is to incorporate direct digital synthesizer (DDS) module at the input of the DAS as shown in Figure (2) to increase the minimum step size. But the main drawback of this technique is large amount of undesired mixing products, which otherwise can be filtered out by using expensive filtering hardware, if small frequency step-size and wide coverage are required goals.

B. Direct Digital Synthesizers (DDS)

Direct Digital Synthesizer scheme allows fine resolution at sub-hertz level but at the cost of limited usable bandwidth and spurious performances. The above limitations can be overcome by using efficient software algorithm and hardware techniques but at the cost of large number of component counts. Figure (3) shows the block diagram of DDS using divider at the output for improved spurious performances.

C. Indirect Frequency Synthesizers (IFS)

Figure (4) shows the typical single-loop IFS using mixer circuit in the feedback path for improved switching speed, phase noise and spurious performances. The drawback of conventional IFS is the degradation in the phase noise performance due to large division ration N, which is required to provide a high frequency output with a fine resolution. In addition to this, IFS is very sensitive to false lock due to the frequency mixing to undesired mixing products. Using fractional divider, overall loop division ratio can be reduced for improved phase noise and tuning speed characteristics. The problem of false locking can be overcome by incorporating DAC to provide sufficiently accurate coarse tuning the VCO to reasonably correct frequency.

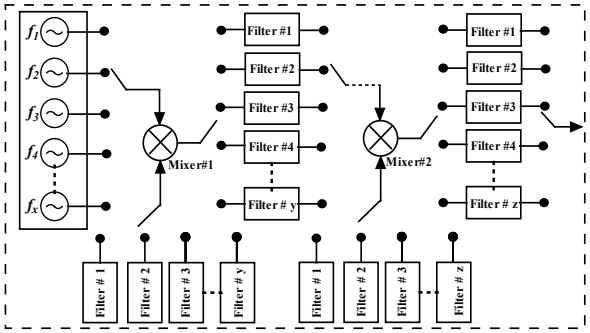

Fig.1. A typical block diagram of the DAS circuit

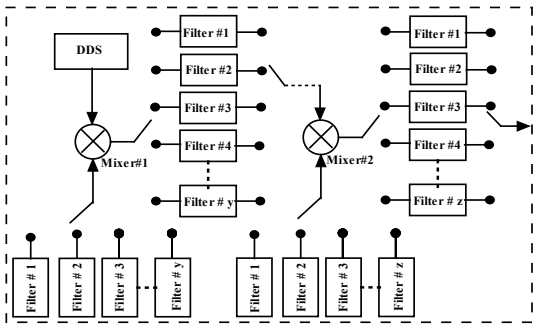

Fig.2. A typical block diagram of the DAS (using DDS at the input)

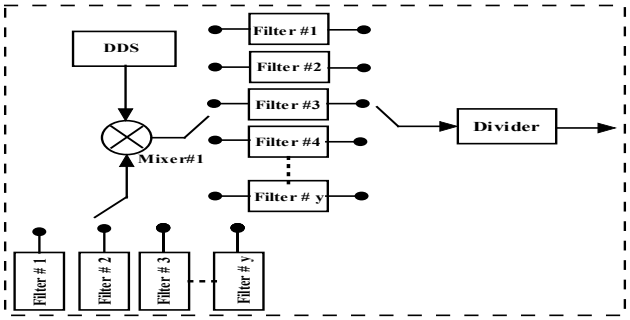

Fig.3 A typical block diagram of the DDS using divider at the output

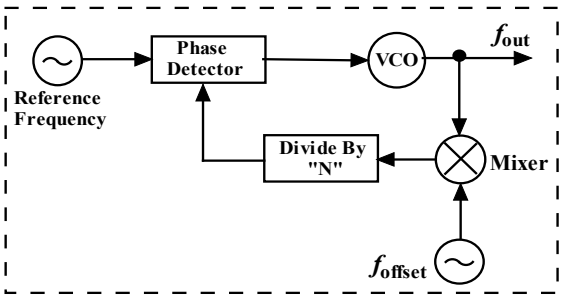

Fig.4 A typical block diagram of the conventional IFS circuit

This acquisition aid needs linear and repeatable tuning characteristics over the operating frequency band and temperature ranges. However, typical DACs are noisy and adversely affect the synthesizer phase noise performance, if they are not properly removed after the initial frequency acquisition [29]. The alternative solution is to use factional-N schemes, which enables a higher phase detector (PD) comparison frequency for a given step-size, resulting, improved phase noise and tuning speed characteristics. However, the main drawback of the fractional-N topology is the high spurious levels due to phase-errors inherent to the fractional division mechanism. In addition to this, IFS architecture is influenced by the VCO characteristics, a prior evaluation of the VCO's characteristics are necessary for high performance IFS solutions. And, due care must be taken while selecting low phase noise and fast switching compatible VCO including DDS module as a fractional divider, inserted into the reference or divider path (Fig. 5). Although, this approach leads to complex hardware structure but offers cost-effective high performance and reasonable priced frequency generation and synthesis solutions for current and later generation communication systems.

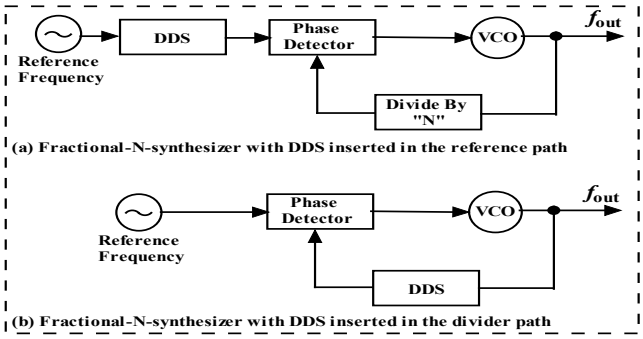

Fig.5. A typical block diagram of the Fractional-N-synthesizer with DDS inserted (a) Reference frequency path and (b) Divider path

III. Low Cost High Performance Synthesizer Solutions

Historically synthesizer designers have relied on YIG oscillators characterizing broadband operation with excellent phase noise performance. The YIG oscillator offers linear tuning characteristics, which simplify the synthesizer coarse-tuning algorithm in multi-loop schemes. These unique features allowed the YIG based synthesizers to dominate over last decades. But YIG oscillators are power hungry and not easily amenable for integration in IC format. The printed resonator based VCO is compatible in IC format but phase noise performance is inferior to YIG counterpart.

The above discussions on reference frequency standard calls for wideband VCOs solutions, the result is evident: the printed resonator VCO described in this paper [Table 1], an potentially achieve faster tuning speed with comparable phase noise and spurious performance without the use of expensive, bulky and power hungry YIG oscillators. Recent progress is in the direction of minimization of system residual noise floor and extending the loop bandwidth to a few megahertz, where printed coupled resonator based solid-state VCO noise becomes competitive with the YIG oscillators. Incorporating high performance hybrid-coupled planar resonator based VCO with a crystal oscillator as a reference gets a cost-effective synthesizer with faster tuning speed.

In addition to this, care must be taken for choice of spectral pure reference frequency sources (Crystal oscillators). The typical phase noise performance of commercially available 100MHz crystal oscillator is –168dBc/Hz at 10 kHz offset from the carrier [25]. The phase noise at 10 kHz offset for 100MHz crystal oscillator can be translated to -128dBc/Hz for a 10 GHz output, which even supersedes the performance of the commercially available low cost YIG oscillators (assuming translation is not affected by the synthesizer system noise floor). As shown in Figure (6), this work addresses the noise minimization mechanism for 155 MHz reference frequency standards using patented active-mode-feedback and noise filtering techniques [1]-[8].

Figure (7) shows the typical measured phase noise plot @ 10 kHz offset, which is better than the commercially available low cost frequency standard.

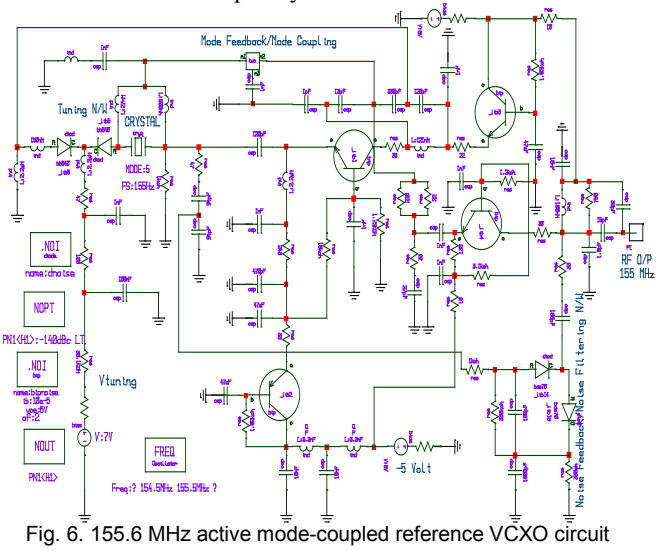

Fig. 6. 155.6 MHz active mode-coupled reference VCXO circuit

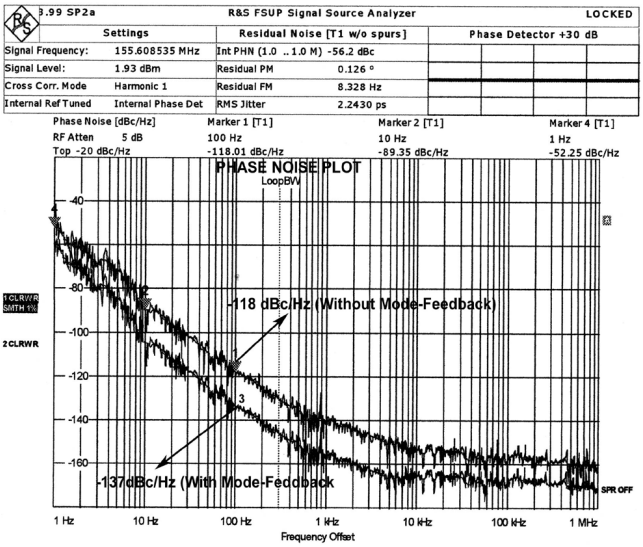

Fig. 7. Measured phase noise plots for 155.6 MHz VCXO (Fig. 6)

Tunable oscillators are instrumental in the operation of many systems, from commercial communications to military radars. Many characteristics define the performance of a tunable RF/microwave oscillator, but one of the more difficult parameters to optimize is phase noise. Because of the importance of bandwidth and phase noise in modern systems, this research work is focused on those two parameters in their innovative line of hybrid-coupled planar resonator (HCPR) oscillators. Figure (8) shows the typical layout of reference frequency standard using evanescent node and extended resonance techniques in HCPR configuration.

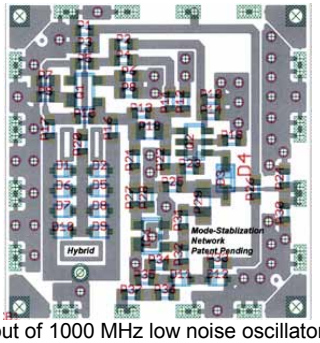

Fig.8. Typical layout of 1000 MHz low noise oscillator (0.5x0.5 inches)

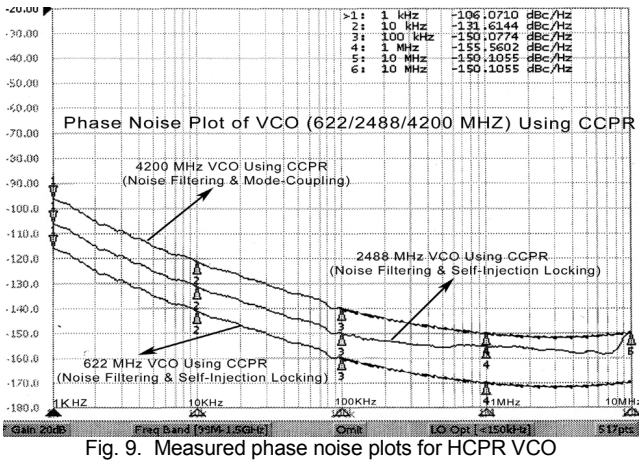

Fig. 9. Measured phase noise plots for HCPR VCO

Figure (9) shows the measured phase noise plot @ 10 kHz offset from the carrier, typical values: –138dBc/Hz (carrier frequency: 622MHz), –128dBc/Hz (carrier frequency: 2488MHz), and –118dBc/Hz (carrier frequency: 4200 MHz); and is not limited to these frequencies. The circuit works at 5V, 20mA, and typical output power is 5 dBm, and second harmonic rejection is better than –20 dBc.

Figure (10) shows the measured phase noise plot for 999.96 MHz spectral pure VCO using HPCR techniques. The typical measured phase noise at 10 kHz offset is -142dBc/Hz, which is state of the art technology in low-cost reference frequency standard in planar technology.

These characteristics, accompanied with the low cost inherent to printed couple resonator based VCO designs (Table 1), are likely to secure their domination in the foreseeable future. Figures (11) and (12) show the block diagram and layout of the HPCR VCOs. The HPCR VCOs (Table 1) are the miniature sources (0.3x0.3 inches) using high Q factor evanescent mode active tunable inductor (ATI) that arm the configurable wideband frequency synthesizers in compact surface-mount packages measuring just 0.6 x 0.6 in. The synthesizers offer wide bandwidths with excellent performance in terms of phase noise, harmonics, settling time, and sideband spurious content, all with low power consumption (5V, 50 mA).

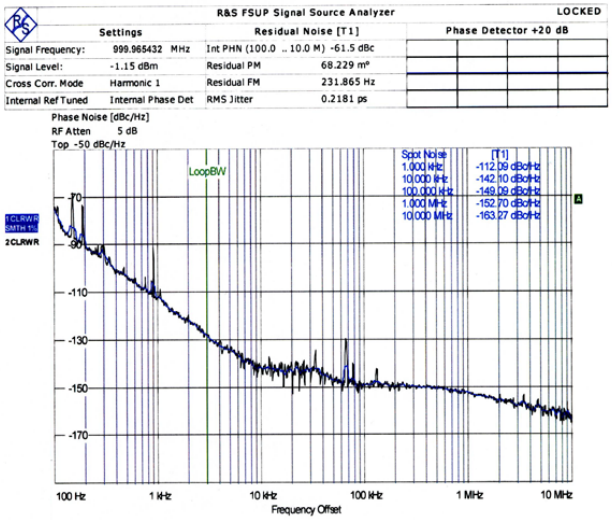

Fig. 10. Measured phase noise plots for 1000 MHz oscillator

Table1: Miniaturized HPCR VCO (0.3 x 0.3 x 0.1 inches)

Frequency (f: MHz)	Tuning: (V)	DC Bias (V, I)	Phase Noise @ 10kHz
100-500 MHz	0.5-28 Volt	5V @ 30 mA	-120 dBc/Hz
500-1500 MHz	0.5-28 Volt	5V @ 30 mA	-110 dBc/Hz
1000-4000 MHz	0.5-28 Volt	5V @ 20 mA	-95 dBc/Hz
4000-8000 MHz	0.5-28 Volt	5V @ 30 mA	-90 dBc/Hz
8000-12000MHz	0.5-28 Volt	5V @ 15 mA	-84 dBc/Hz
12000-16000 MHz	0.5-28 Volt	5V @ 25 mA	-78 dBc/Hz
16000-18000 MHz	0.5-28 Volt	5V @ 30 mA	-73 dBc/Hz

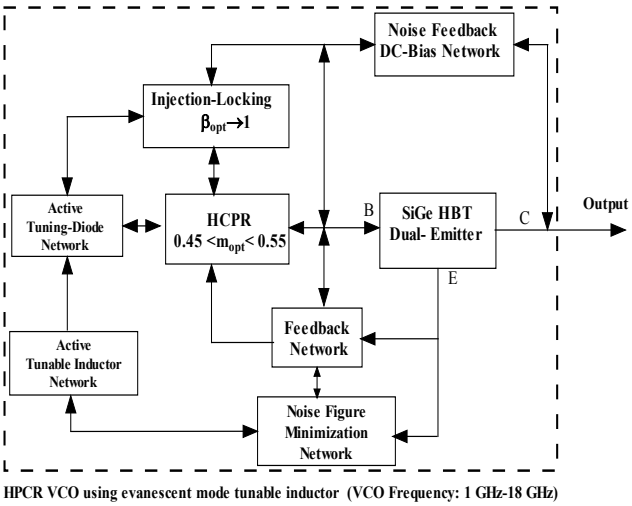

Fig.11. Block diagram of miniaturized VCO (0.3x0.3x0.1 inches)

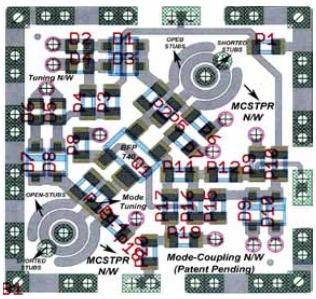

Fig.12. Layout of HPCR ATI VCO ((0.3x0.3x0.1 inches) (Fig. 11)

IV. High-Q Factor Hybrid- Coipled Planar Resonators

The Q (quality) factor of the coupled planar resonator network can be enhanced by introducing optimum coupling mechanism (electric/magnetic/hybrid). Figure (13) illustrates the layout of the typical electric, magnetic, hybrid-coupling planar resonator networks, and oscillator circuits for comparative analysis [24].

As described in Figure (13), the coupling dynamics can be characterized by proximity effect through the fringing fields, which exponentially decays outside the region; electric and magnetic field intensity tends to concentrate near the side having maximum field distribution. The coupling factor β (β_e: electric, β_m: magnetic and β_h: hybrid) can be described as

$$\beta_e \cong \frac{coupled-electrical\quad energy}{stored-energy\ of\ uncoupled-resonator} \cong \frac{f_{me}^2 - f_{ee}^2}{f_{me}^2 + f_{ee}^2} \cong \frac{C_{me}}{C} \quad (1)$$

$$\beta_m \cong \frac{coupled-magnetic\quad energy}{stored-energy\ of\ uncoupled-resonator} \cong \frac{f_{em}^2 - f_{mm}^2}{f_{em}^2 + f_{mm}^2} \cong \frac{L_{mm}}{L} \quad (2)$$

$$\beta_h \cong \frac{coupled-electro-magnetic\quad energy}{stored-energy\ of\ uncoupled-resonator} \cong \frac{f_{eh}^2 - f_{mh}^2}{f_{eh}^2 + f_{mh}^2} \cong \frac{CL_{mh} + LC_{mh}}{LC + L_{mh}C_{mh}} \quad (3)$$

where

$f_{ee} = \frac{1}{2\pi\sqrt{L(C+C_{me})}}$, $f_{me} = \frac{1}{2\pi\sqrt{L(C-C_{me})}}$, C_{me}: Mutual Capacitance

$f_{em} = \frac{1}{2\pi\sqrt{C(L-L_m)}}$, $f_{mm} = \frac{1}{2\pi\sqrt{C(L+L_m)}}$, L_{mm}: Mutual Inductance

$f_{eh}=\frac{1}{2\pi\sqrt{(L-L_{mh})(C-C_{mh})}}$, $f_{mh}=\frac{1}{2\pi\sqrt{(L+L_{mh})(C+C_{mh})}}$, L_{mh}: Hybrid Inductance

$f_0=\frac{1}{2\pi\sqrt{LC}}$, f_0: Fundamental resonance frequency of uncoupled resonator. The loaded quality factor Q_L of the coupled resonator network is given in terms of unloaded quality factor Q_o as [24]

$$Q_L(\omega_0)=\frac{\omega_0}{2}\left[\frac{\partial\phi}{\partial\omega}\right] \quad (5)$$

$$[Q_L(\omega_0)]_{electrical-coupling}\cong 2\left[\frac{Q_0}{(1+\beta_e)}\right]_{\beta_e<<1}\cong 2Q_0 \quad (6)$$

$$[Q_L(\omega_0)]_{magnetical-coupling}\cong 2[Q_0(1+\beta_m)]_{\beta\to 1}\cong 2Q_0 \quad (7)$$

$$[Q_L(\omega_0)]_{hybrid-coupling}\cong 2\left[Q_0\frac{(1+\beta_{mh})}{(1+\beta_{eh})}\right]_{\beta_e<<1,\ \beta_m\to 1}\cong 2Q_0 \quad (8)$$

where $\frac{\partial\phi}{\partial\omega}$ is the rate of change of the phase, and Q_0 is the unloaded Q-factor of the uncoupled single open loop microstrip line resonator (Fig. 13). From (6), (7), and (8), there is trade-off between improving the Q factor and the permissible attenuation required (which is compensated by active device for oscillation build up). The coupling mechanism described in

Figure (13) shows improvement in quality factor in comparison to single uncoupled planar resonator but drawback is limited tuning range (less than 1%). From (6), (7) and (8), loaded quality factor (Q_L) can be maximized by either lowering the value of mutual capacitance (C_m) and inductance (L_m) or maximizing the self-capacitance (C) and inductance (L), therefore, upper limit of the loaded Q- factor is dependent on the coupling β that can optimized by controlling the width of the transmission line (w), gap of the open line resonator (p), and spacing between the two open line resonators (d).

However, dynamic controlling and tuning the parameters w, p, and d at high frequency in IC technology is challenging task. For wideband tunability, the coupling factor β_j has to be dynamically tuned for low phase noise performances over the operating frequency band. The simplified approach for realization of dynamically controlled coupling factor β_j can be achieved by incorporating active tunable inductor (ATI) as a coupling and tuning mechanism across coupled resonators.

V. Noise Dynmaics And Phase Noise Analysis

The expression of phase noise can be given by [11, pp. 332]

$$\pounds(f_m)=10\log\left\{\left[1+\frac{f_0^{\,2}}{(2f_mQ_L)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0}+\frac{2kTRK_0^{\,2}}{f_m^{\,2}}\right\} \quad (9)$$

$$\pounds(f_m)=10\log\left\{\left[1+\frac{f_0^{\,2}}{(2f_mQ_0)^2m^2(1-m)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0}+\frac{2kTRK_0^{\,2}}{f_m^{\,2}}\right\} \quad (10)$$

where $\pounds(f_m)$, f_m, f_0, f_c, Q_L, Q_0, F, k, T, P_o, R, m and K_0 are the ratio of the sideband power in a 1Hz bandwidth at f_m to total power in dB, offset frequency, flicker corner frequency, loaded Q, unloaded Q, noise factor, Boltzman's constant, temperature in degree Kelvin, average output power, equivalent noise resistance of tuning diode, ratio of the loaded and unloaded quality factor and voltage gain. From (6), (7) and (8), m is given in terms of coupling coefficient as

$$m=\frac{Q_L}{Q_0}\cong\left[\frac{2}{(1+\beta_e)}\right]_{electrical}\cong[2(1+\beta_m)]_{magnetic}\cong\left[\frac{2(1+\beta_{mh})}{(1+\beta_{eh})}\right]_{hybrid} \quad (11)$$

By differentiating (10), with respect to m and equating to zero, local minimum value of phase noise for a given resonator and oscillator topology can be given by

$$\frac{\partial^2}{\partial m^2}[\pounds(f_m)]_{m=m_{opt}}=0\Rightarrow$$

$$\frac{d^2}{dm^2}\left[10\log\left\{\left[1+\frac{f_0^{\,2}}{(2f_mQ_0)^2m^2(1-m)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0}+\frac{2kTRK_0^{\,2}}{f_m^{\,2}}\right\}\right]=0\Rightarrow m_{opt}=0.5 \quad (12)$$

$$m_{opt}\to 0.5\ \Rightarrow\ [\beta_e]_{opt}<<1,\ \ [\beta_m]_{opt}\to 1,\ \ 0<[\beta_h]_{opt}<1 \quad (13)$$

From (13), for low phase noise applications, m_{opt} and β_{opt} should be dynamically tuned and must converge in the vicinity of $m_{opt}\cong 0.5$ and $0<\beta_{opt}<1$ respectively for best phase noise performances. As an example for validation, Figure (14) shows the typical layout of the fixed frequency 18 GHz active planar coupled VCOs using a SiGe hetrojunction-bipolar-transistor (HBT), fabricated on Rogers substrate material with a dielectric constant of 3.38 and thickness of 30mils (microstripline/stripline) for the validation of the new approach (dynamically controlling m_{opt} and β_{opt} for minimum noise figure).

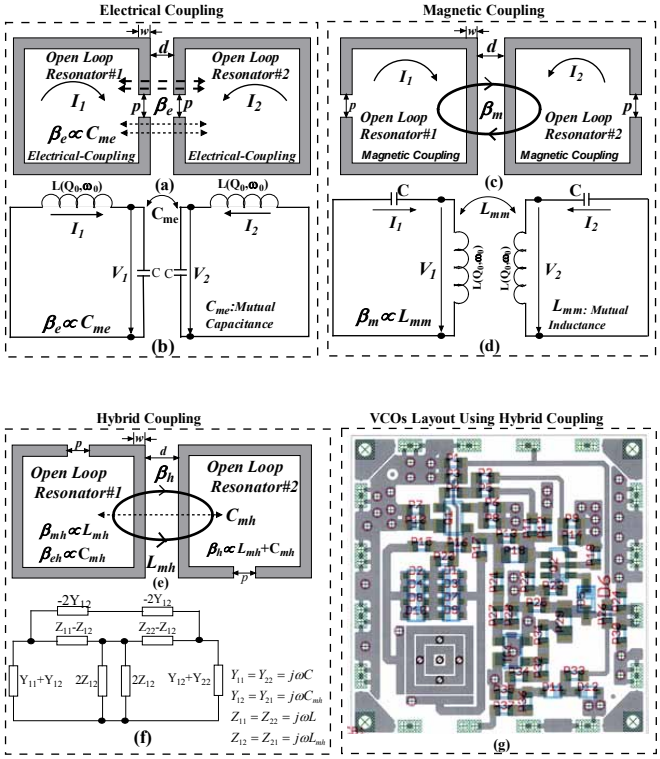

Fig.13. Typical simplified structure of open loop microstrip line coupled resonator networks:(a) Electrical coupling, (b) Equivalent lumped model of electrical coupling, (c) Magnetic coupling, (d) Equivalent lumped model of magnetic coupling, (e) Hybrid coupling, (f) Equivalent lumped model of hybrid coupling and (g) Layout of VCO using electric and magnetic coupling.

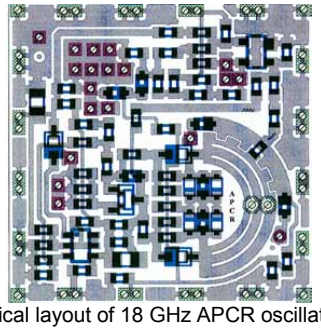

Fig.14. A typical layout of 18 GHz APCR oscillator using ATI

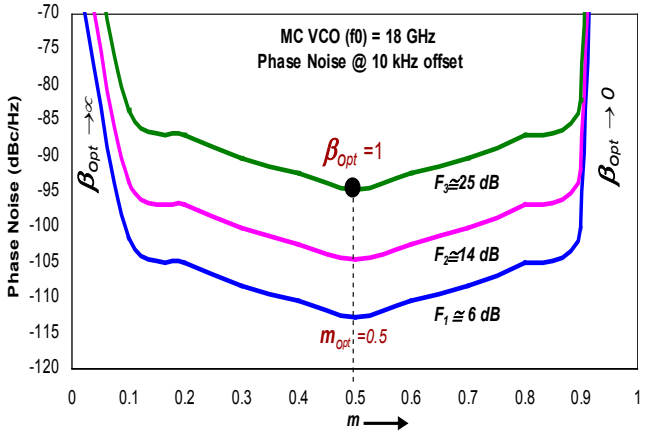

Fig. 15. Simulated phase noise plot of MC VCO with respect to m_{opt},

Figure (15) shows the CAD simulated phase noise plot for a 18 GHz APCR VCO (Fig. 14) at offset 10 kHz from the carrier with respect to m_{opt} and β_{opt}.

Figure (16) shows the measured phase noise plot of the discrete version of the high Q active tunable inductor (ATI) based HPCR VCO (which is planar and amenable to a MMIC manufacturing process), typically – 110 dBc/Hz @ 10 kHz from the carrier that agrees within 3-4 dB of the CAD simulated results.

The new MFSH series of compact and configurable frequency synthesizers [Table 2] take advantage of the small size and performance VCOs [Table 1] to provide synthesized performance in a SMD package measuring just 0.6 x 0.6 in.

VI. Configurable Frequency Synthesizers

Technologies for creating frequency synthesizers are diverse, from traditional analog methods using PLLs to direct digital synthesizers (DDS) that rely on high-speed digital–to-analog converters (DACs) to transform digital input words into analog output signals. Frequency synthesizers can be categorized into mainly three groups: analogue, digital or mixed signal (hybrid). The frequency synthesizer described in this paper falls into the hybrid category.

The block diagram for a typical MFSH frequency synthesizer (Fig. 17) includes a VCO, PLL, IC, charge pump, loop filter, amplifier, and voltage regulator. A typical unit, [Table 2], tunes from 3000 to 6000 MHz in 1-MHz steps with settling time of less than 1 ms and phase noise of -85 dBc/Hz offset 10 kHz from the carrier and -110dBc/Hz offset 100 kHz from the carrier.

The synthesizer draws typically less than 50 mA current from a 5-V supply. Although the integrated VCOs are very small in size and offer Pick-N-Place features but leaves much to be desired (current consumption and phase noise).

In addition, most of these integrated synthesizers require external resonator and filtering network for compensation of frequency drift due to notorious tolerances cause due to onboard associated tuning diode. The risk factor associated with this solution is alarming since optimizations and changes during the design phase can be expensive and time consuming.

On the contrary, HPCR VCO series [Table 1] offers a realistic option in size to IC oscillators, including overall performances. In addition to this, VCO series [Table 1] provide configurable solutions (user-definable operating frequency and tuning range in same foot print and size that allows system designer freedom to Pick-N-Place HPCR VCOs module).

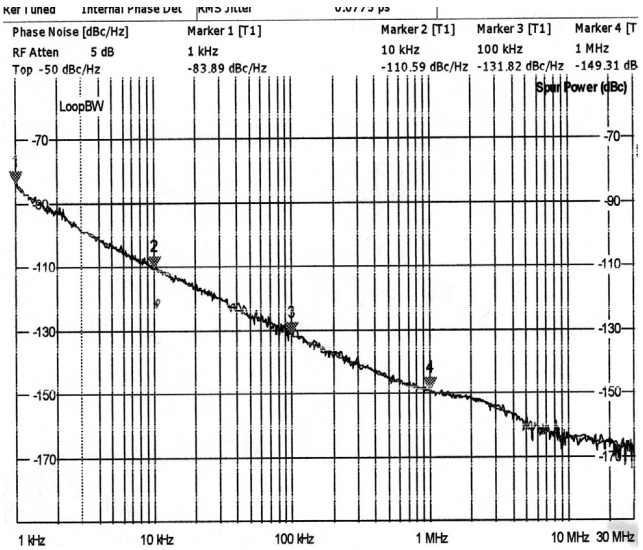

Fig.16. Measured phase noise plot of 18 GHz APCR VCO using ATI

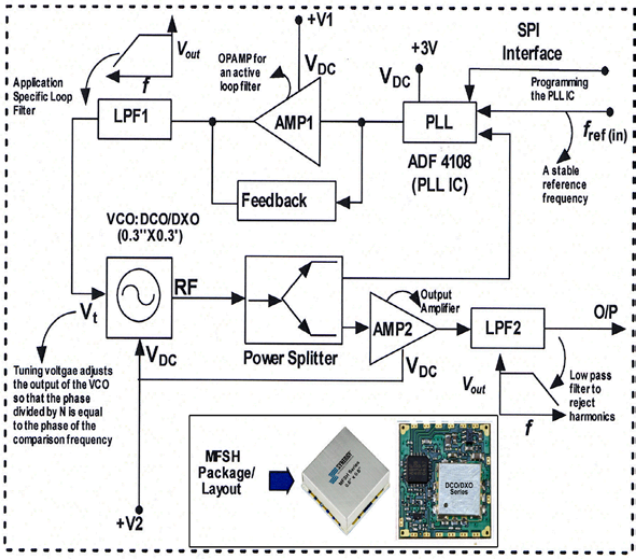

Fig.17. Block diagram of configurable synthesizer (MFSH series)

Table 2: Compact and Configurable Synthesizers (0.6x0.6 inches)

Frequency	Step Size	O/P Power	PN @ 10kHz
1-4 GHz	1000 kHz	+0 dBm	-86 dBc/Hz
2-4 GHz	1000 kHz	+1 dBm	-90 dBc/Hz
3-6 GHz	1000 kHz	-3 dBm	-85 dBc/Hz
4-8 GHz	1000 kHz	-3 dBm	-82 dBc/Hz

The tiny HPCR VCOs [Table 1] are designed to simplify modular integration for high performance inexpensive frequency generations and synthesis circuit for modern communication systems.

The synthesizer topology using HPCR VCO can operate as low as 100 MHz with some fundamental changes in the basic oscillator design. The planar-resonator oscillator/synthesizer technology is currently produced in discrete-device form, but is amenable for use in VCO and frequency synthesizer ICs and monolithic-microwave integrated circuits (MMICs).

Shrinking the size of planar resonators has led to extremely compact oscillators that are the building blocks for tiny, high-performance, PLL-based frequency synthesizers. Competing available semiconductor technologies may not deliver the same level performance in terms of cost, size, and power.

VII. Conclusion

The reported miniaturized VCOs overcome the limitation of the past attempt to combine phase-locked-loop (PLL) in tiny package (0.6 x 0.6 inches) for multi-band and multi-mode operations hybrid coupling mechanism. Shrinking the size of planar resonators employing has led to tiny (0.3 x 0.3 inches) VCOs that arms the low-cost and configurable synthesizers.

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